

# SSC8L3410JN4

## **Dual N-Channel Enhancement MOSFET**

#### Features

V <sub>DS</sub>	V <sub>GS</sub>	R <sub>DS(ON)</sub> Typ.	ID
40V	±20V	5.8mΩ@10V	45A
	<u> </u>	8.3mΩ@4V5	437

#### > Description

The SSC8L3410JN4 is N-Channel enhancement mode MOSFET. Uses SGT Technology and design to provide excellent RDSON with low gate charge. This device is suitable for use in DC - DC conversion, power switch and charging circuit.

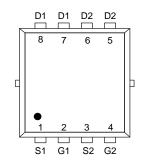
100% UIS + ΔVDS + Rg Tested!

- > Applications
- Inverter
- DC-DC Converter
- Half and Full Bridge Topology
- Motor Drive Control

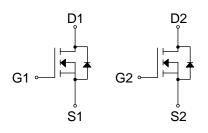
#### > Ordering Information

Device	Package	Shipping
SSC8L3410JN4	PDFN3.3X3.3-8L	5000/Reel

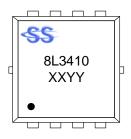
### Pin configuration



#### PDFN3.3x3.3-8L (Top View)



**Pin Configuration** 



#### <u>Marking</u>

(XXYY: Internal Traceability Code)



Symbol	Parameter		Ratings	Unit
VDSS	Drain-to-Source Voltage		40	V
V <sub>GSS</sub>	Gate-to-Source Volt	age	±20	V
	Ocationary Desir Organith	Tc = 25℃	45	A
ID	Continuous Drain Current <sup> b</sup>	Tc=100℃	24	A
Ідм	Pulsed Drain Curre	nt <sup>b</sup>	190	А
I <sub>DSM</sub> Continuous Drain Current <sup>a</sup>	T <sub>A</sub> = 25℃	20	А	
IDSM	Continuous Drain Current a	'oltage       40         'oltage $\pm 20$ $T_c = 25^{\circ}C$ 45 $T_c = 100^{\circ}C$ 24         trent b       190 $T_A = 25^{\circ}C$ 20 $T_A = 70^{\circ}C$ 8 $T_c = 100^{\circ}C$ 8.6 $T_c = 100^{\circ}C$ 8.6 $T_A = 70^{\circ}C$ 1.45 $= 0.5mH$ 16         .= 0.5mH       64         mperature       -55 to 150	8	А
5	During Director (inc.)	Tc=25℃	21	W
P <sub>D</sub>	Power Dissipation °	Tc = 100℃	8.6	W
<u> </u>	Duran Dia institut a	T <sub>A</sub> =25℃	2.3	W
Pdsm	Power Dissipation <sup>a</sup>	$T_c = 25^{\circ}C$ $T_c = 100^{\circ}C$ rrrent b $T_A = 25^{\circ}C$ $T_c = 25^{\circ}C$ $T_c = 25^{\circ}C$ $T_c = 100^{\circ}C$ $T_A = 25^{\circ}C$ $T_A = 70^{\circ}C$ $T_A = 70^{\circ}C$ $L = 0.5mH$	1.45	W
I <sub>AS</sub>	Avalanche Current <sup>b</sup> L = 0.5mH		16	Α
E <sub>AS</sub>	Avalanche Energy♭L = 0.5mH		64	mJ
TJ	Operation junction temp	Operation junction temperature		°C
Tstg	Storage temperature	range	-55 to 150	°C

#### ➤ Absolute Maximum Ratings (T<sub>A</sub>=25°C unless otherwise noted)

### > Thermal Resistance Ratings (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit	
Reja	Junction-to-Ambient Thermal Resistance <sup>a</sup>	55		
Rejc	Junction-to-Case Thermal Resistance	5.8	℃/W	

Note:

- a. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper,in a still air environment with T<sub>A</sub>=25 °C. The value in any given application depends on the user is specific board design. The current rating is based on the t≤10s thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- d. The maximum current rating is package limited.



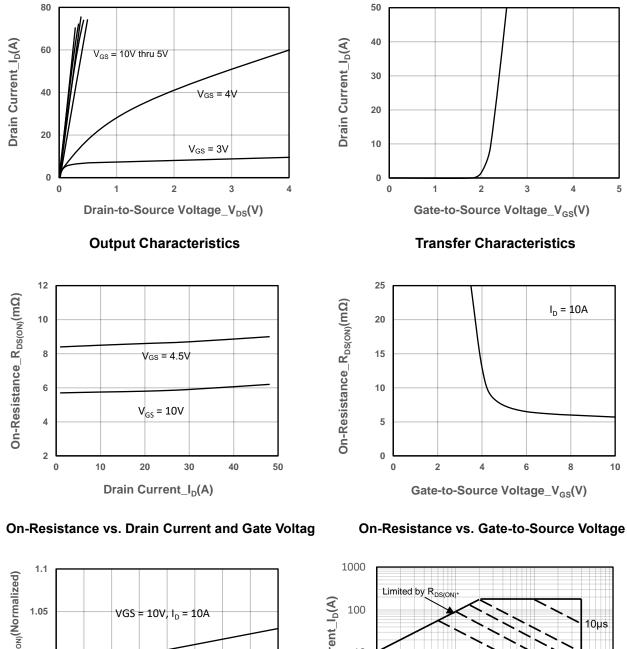


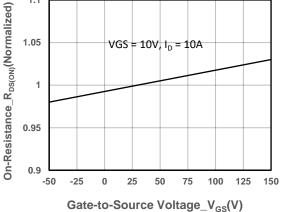
# $\succ$ Electrical Characteristics (T<sub>A</sub>=25 °C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250µA	40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 uA$	1	1.6	2.5	V
Drain-Source On-Resistance	D	V <sub>GS</sub> = 10V, I <sub>D</sub> = 12A		5.8	7.5	
Drain-Source On-Resistance	$R_{DS(on)}$	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 10A		8.3	11	mΩ
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V			1	μA
Gate-Source Leak Current	lgss	$V_{GS}$ = ±20V, $V_{DS}$ = 0V			±100	nA
Forward Voltage	$V_{\text{SD}}$	V <sub>GS</sub> = 0V, I <sub>S</sub> = 1A			1.2	V
Gate Resistance	Rg	V <sub>DS</sub> = 0V, f = 1MHz		3.7		Ω
Input Capacitance	Ciss			648		
Output Capacitance	Coss	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, - f = 1MHz -		360		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			17		
Total Gate Charge	QG			11.5		
Gate to Source Charge	Q <sub>GS</sub>	$V_{GS} = 10V, V_{DS} = 20V,$ $I_{D} = 12A$		2.1		nC
Gate to Drain Charge	$Q_{GD}$	$I_D - IZA$		2.2		
Turn-on Delay Time	T <sub>D(ON)</sub>			8		
Rise Time	Tr	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 15V,		6		
Turn-off Delay Time	T <sub>D(OFF)</sub>	I <sub>D</sub> = 1A, R <sub>G</sub> = 3.3Ω		34		ns
Fall Time	T <sub>f</sub>			10		
Diode Recovery Time	Trr	I⊧=20A, di/dt=500A/us		25		ns
Diode Recovery Charge	Qrr	I⊧=20A, di/dt=500A/us		60		nC

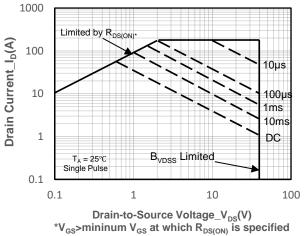


#### Typical Performance Characteristics (T<sub>A</sub>=25℃ unless otherwise noted) $\triangleright$





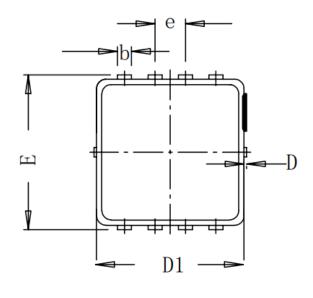
**On-Resistance vs. Junction Temperature** 

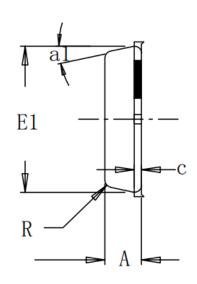


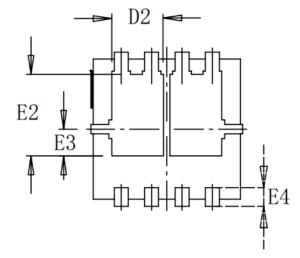
#### Safe Operating Area vs. Junction-to-Ambient



# > Package Information







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SYMBOL	MILLIMETER		
SIMDUL	MIN	NOM	MAX
٨	0.75	0.78	0.81
b	0.297	0.3	0.35
C	-	0.152	-
D	0.00	0.05	0.1
D1	3.12	3.15	3.18
D2	-	1.05	-
E	32	33	3.4
El	3.09	3.12	3.15
E2	-	1.75	
E3	-	0.575	-
E4	-	0.4	
R	-	0.15	
e	0.6		
al	-	12"	



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